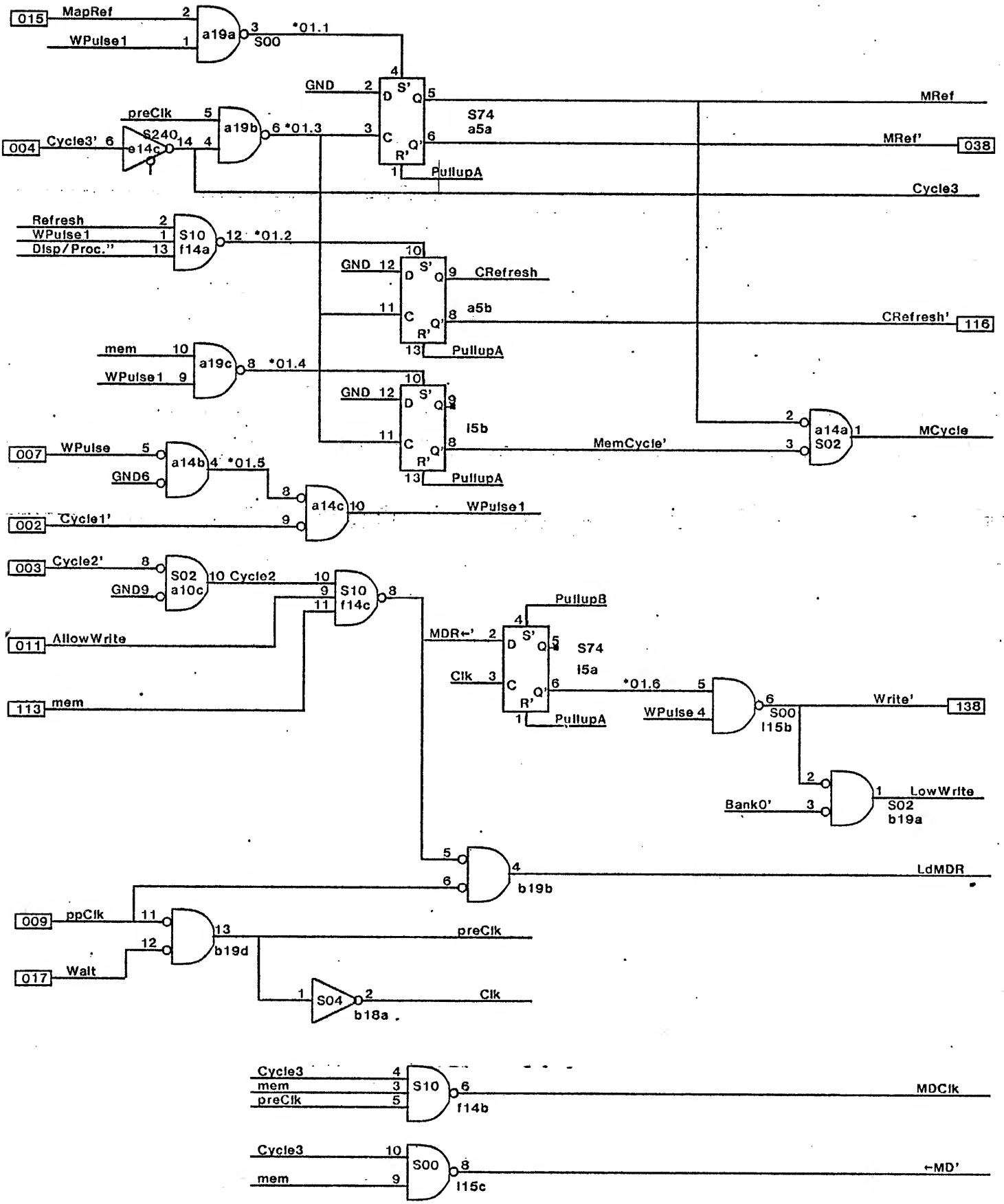
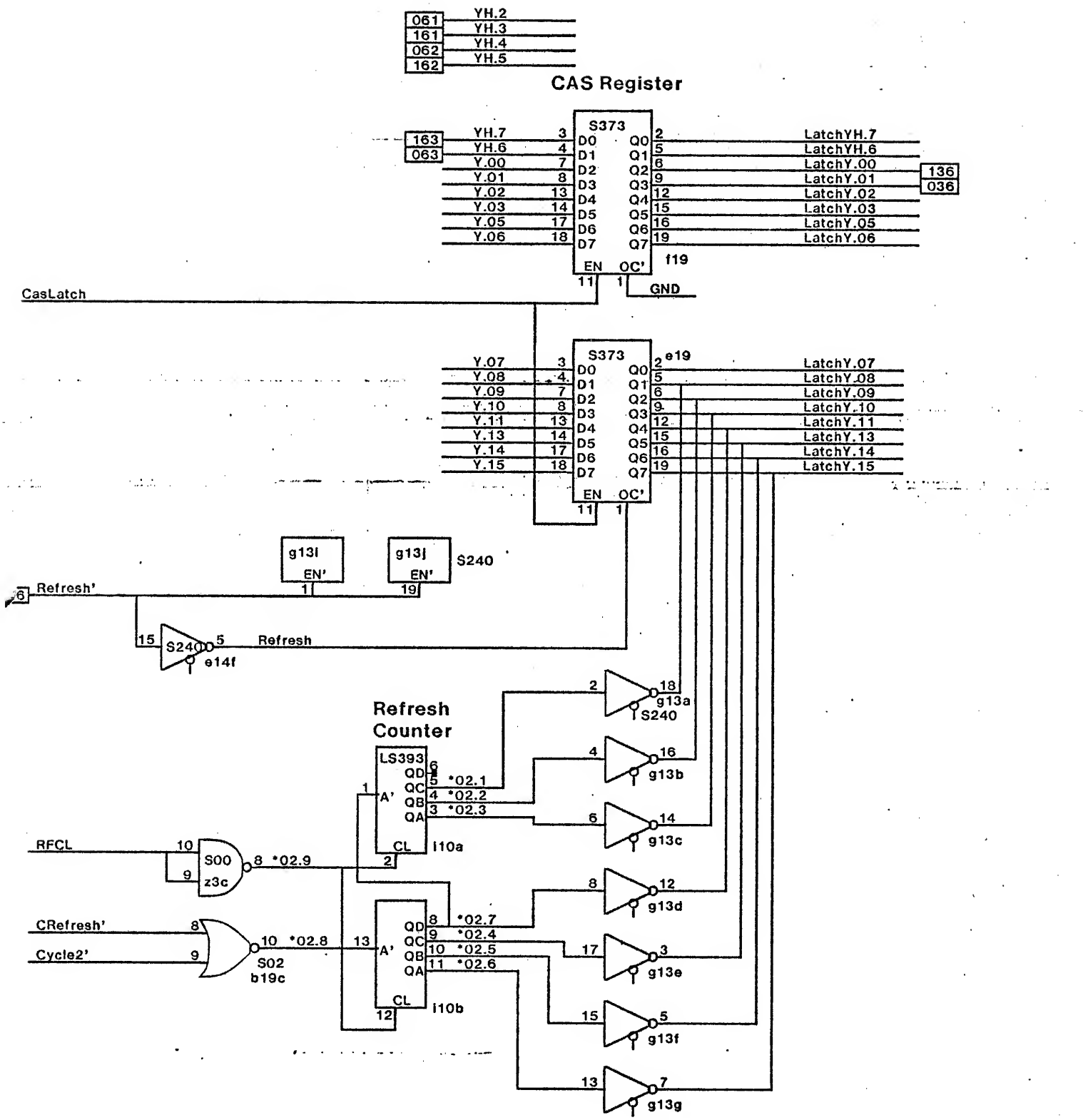
Memory Control Card

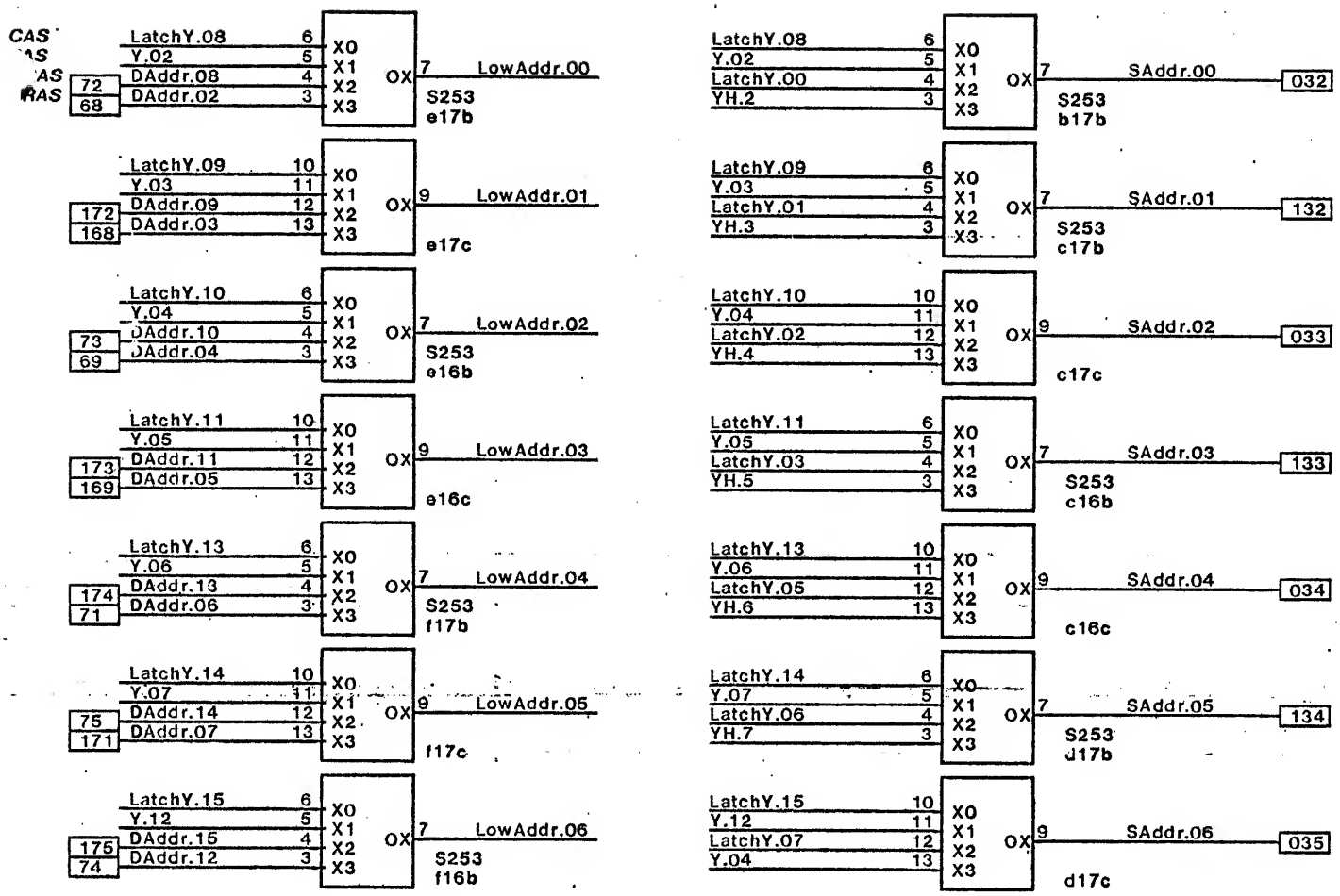
1. Write, CRefresh', MRef, LdMDR, Cycle Rcv., MDClk, ←MD'
2. Refresh Counter & Cas Registers
3. Address Selection Logic, RASDly, & LRASDly
4. Memory Bank Selection
5. Drivers for Address, CAS', & Write'
6. Low Bank A
7. Low Bank B
8. Low Bank C
9. Low Bank D
10. Mem. Data Register, Mem. Control Reg., Check bit Gen.
11. Memory Chip data paths
12. Memory Data Buffers
13. Syndrome Generator
14. Error Correction Data paths
15. Error Log Register
16. Resistors and R-Dips
17. Caps Diodes and Fuses
18. Test Points
19. Material List
20. Board Layout



XEROX SDD	Project WS	Write,CRefresh',MRef,LdMDR, CycleRcv. MDClk,←MD'	File EMCTL01.sil	Designer Crane	Rev D	Date 3/19/80	Page 1

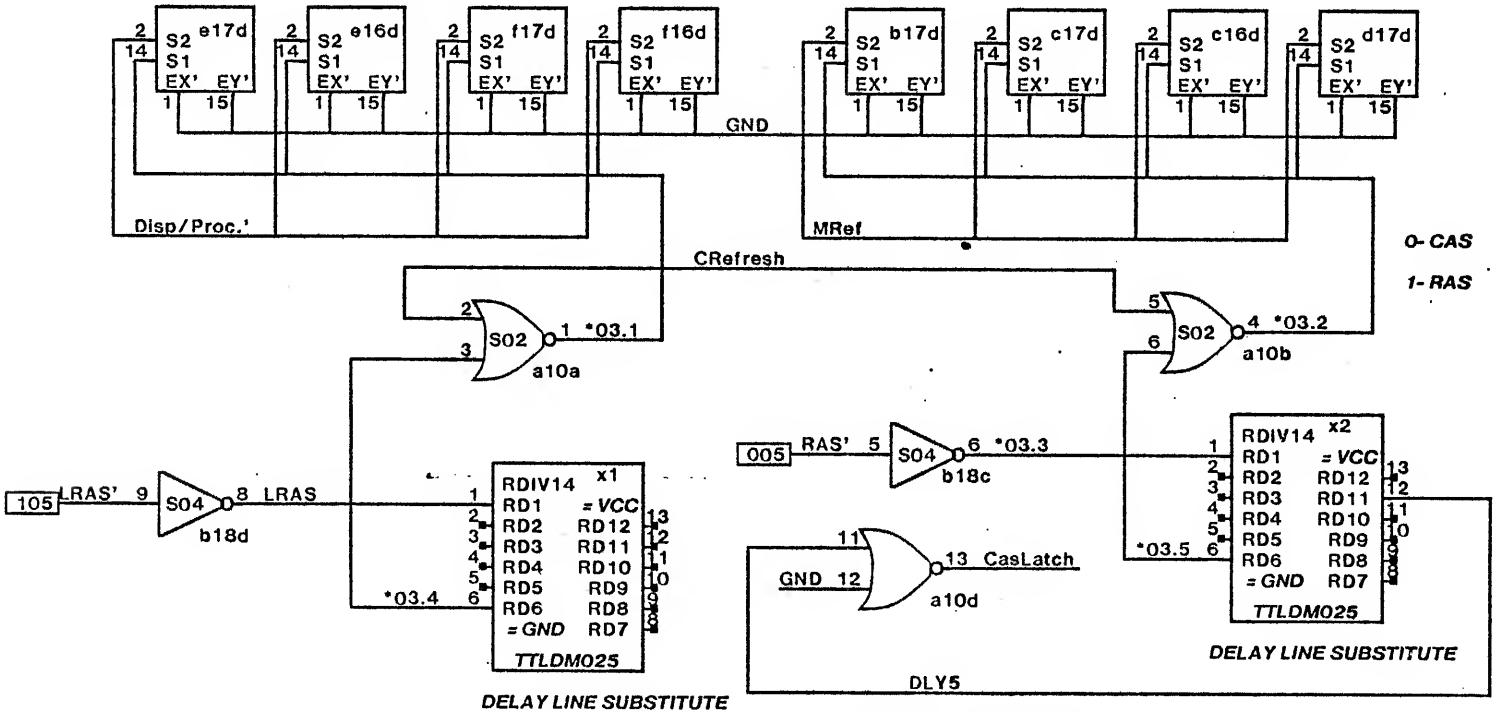


XEROX SDD	Project WS	Refresh Counter & CAS Registers	File EMCTL02.sil	Designer Crane	Rev D	Date 2/14/80	Page 2

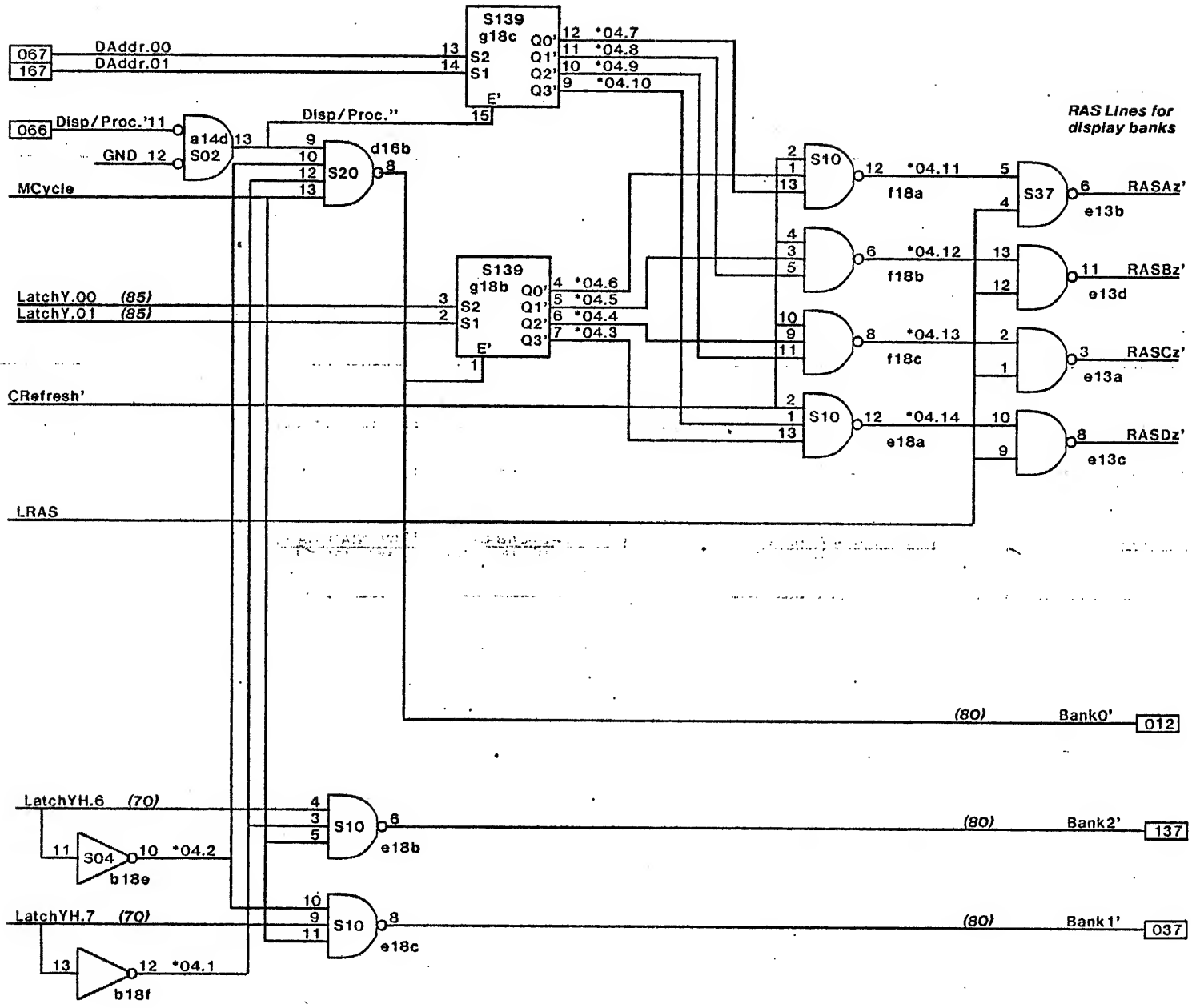


Low Bank Selection

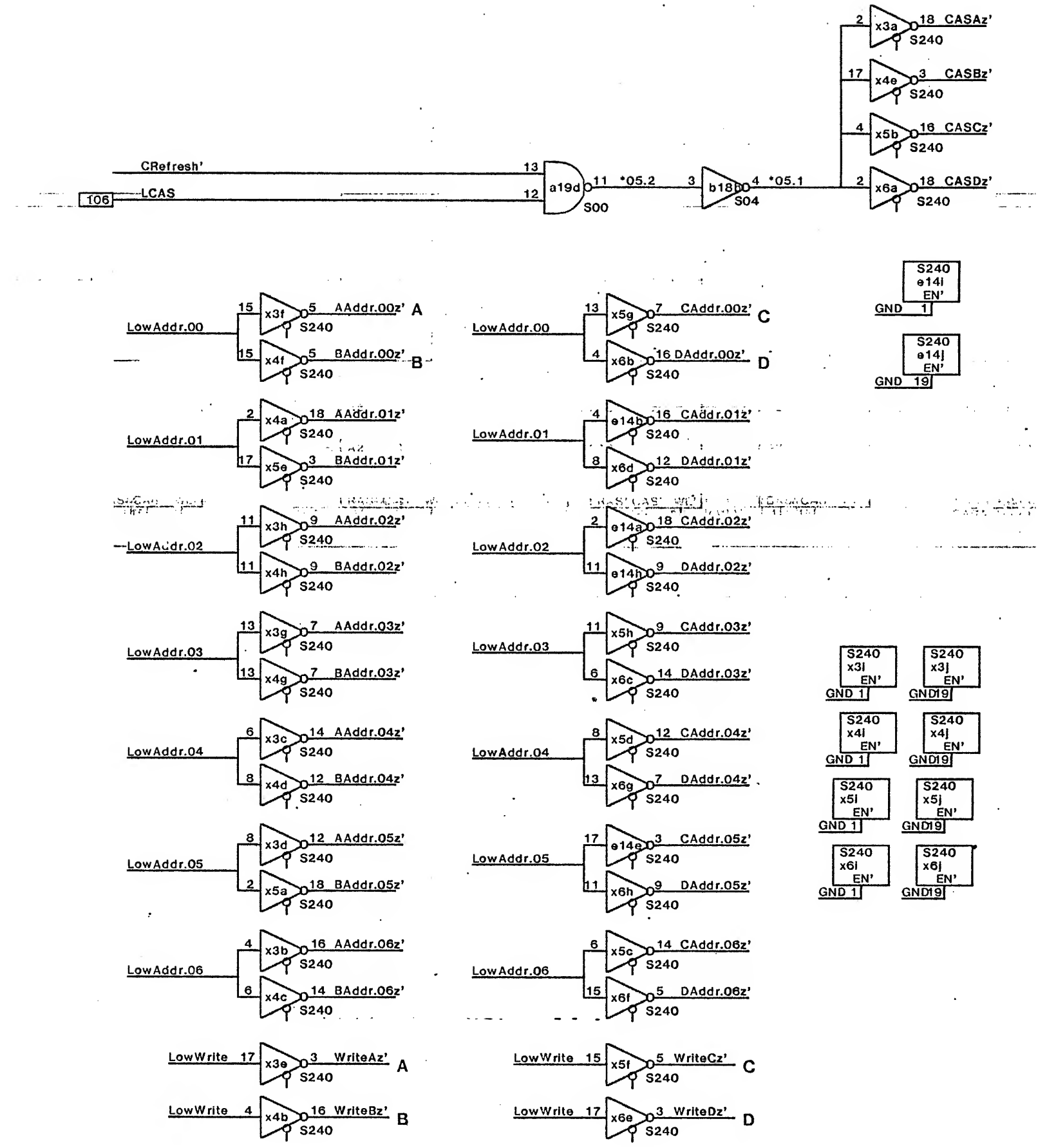
High Bank Selection



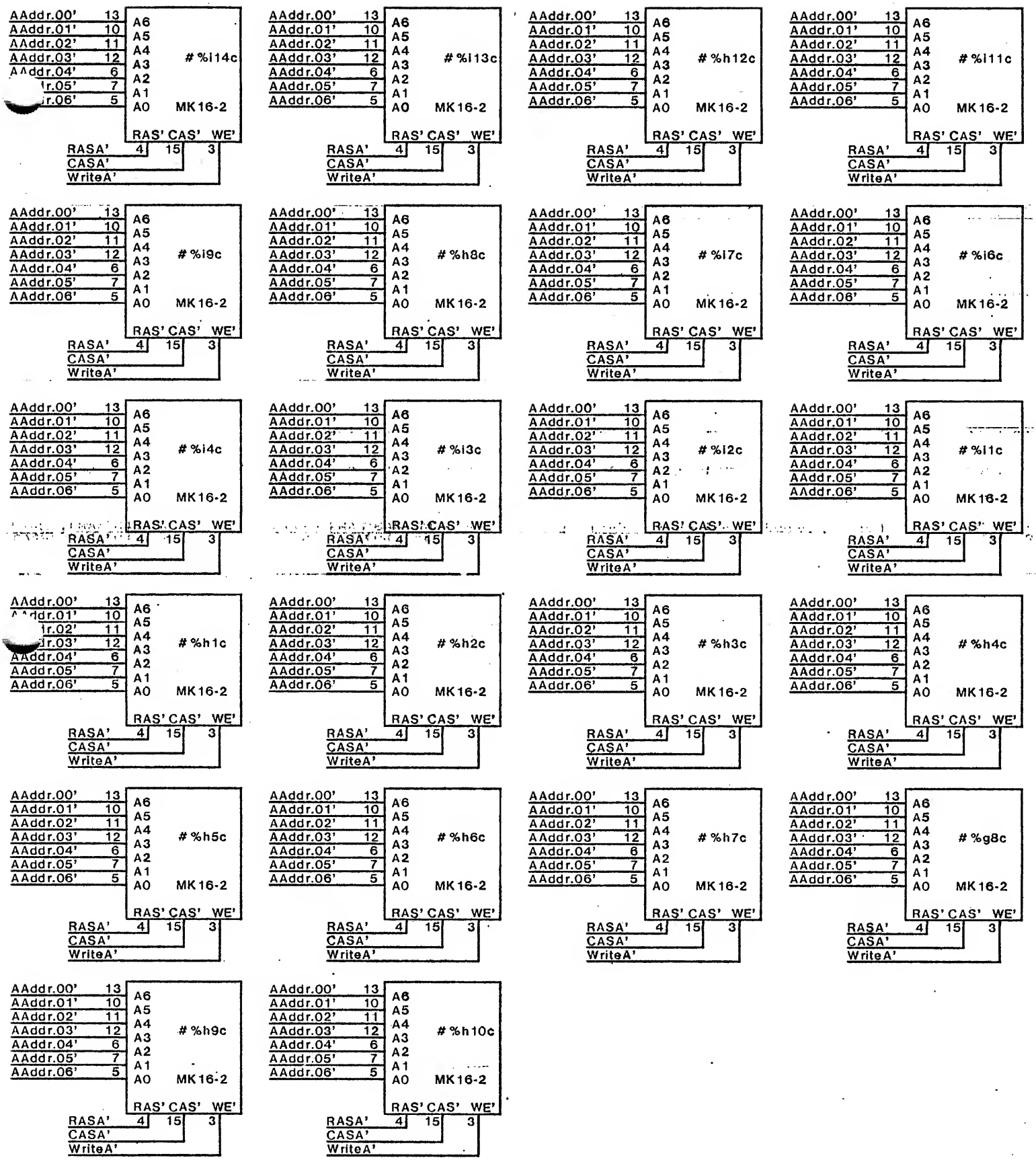
XEROX SDD	Project WS	Address Selection Logic RASDly & LRASDly	File EMCTL03.sil	Designer Crane	Rev D	Date 3/19/80	Page 3



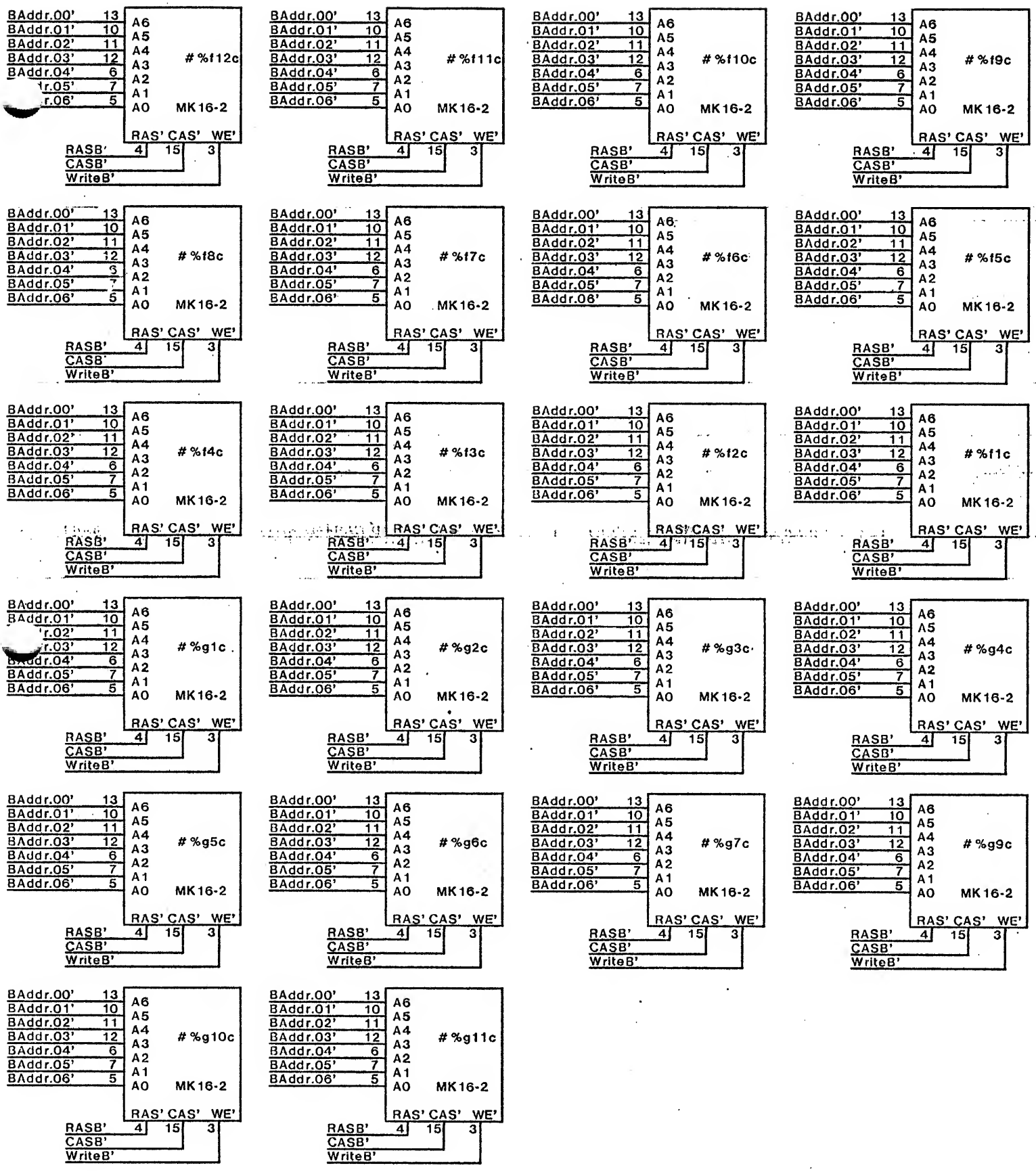
XEROX SDD	Project WS	Memory Bank Selection	File EMCTL04.sil	Designer Crane	Rev D	Date 3/19/80	Page 4



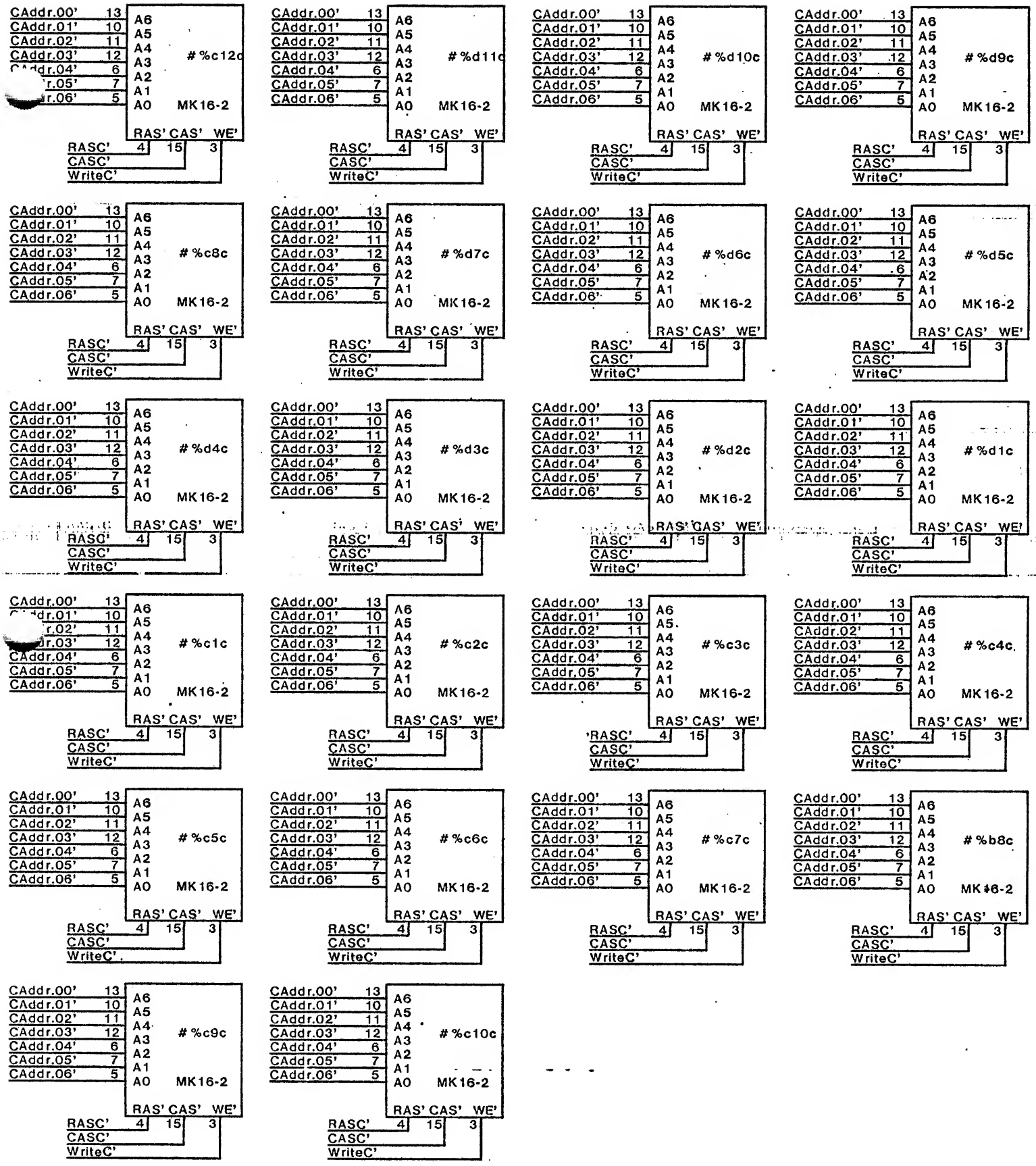
XEROX SDD	Project WS	Low 64K Bank Drivers for Address, CAS', & Write'	File EMCTL05.sil	Designer Crane/Cucinitti	Rev D	Date 3/19/80	Page 5



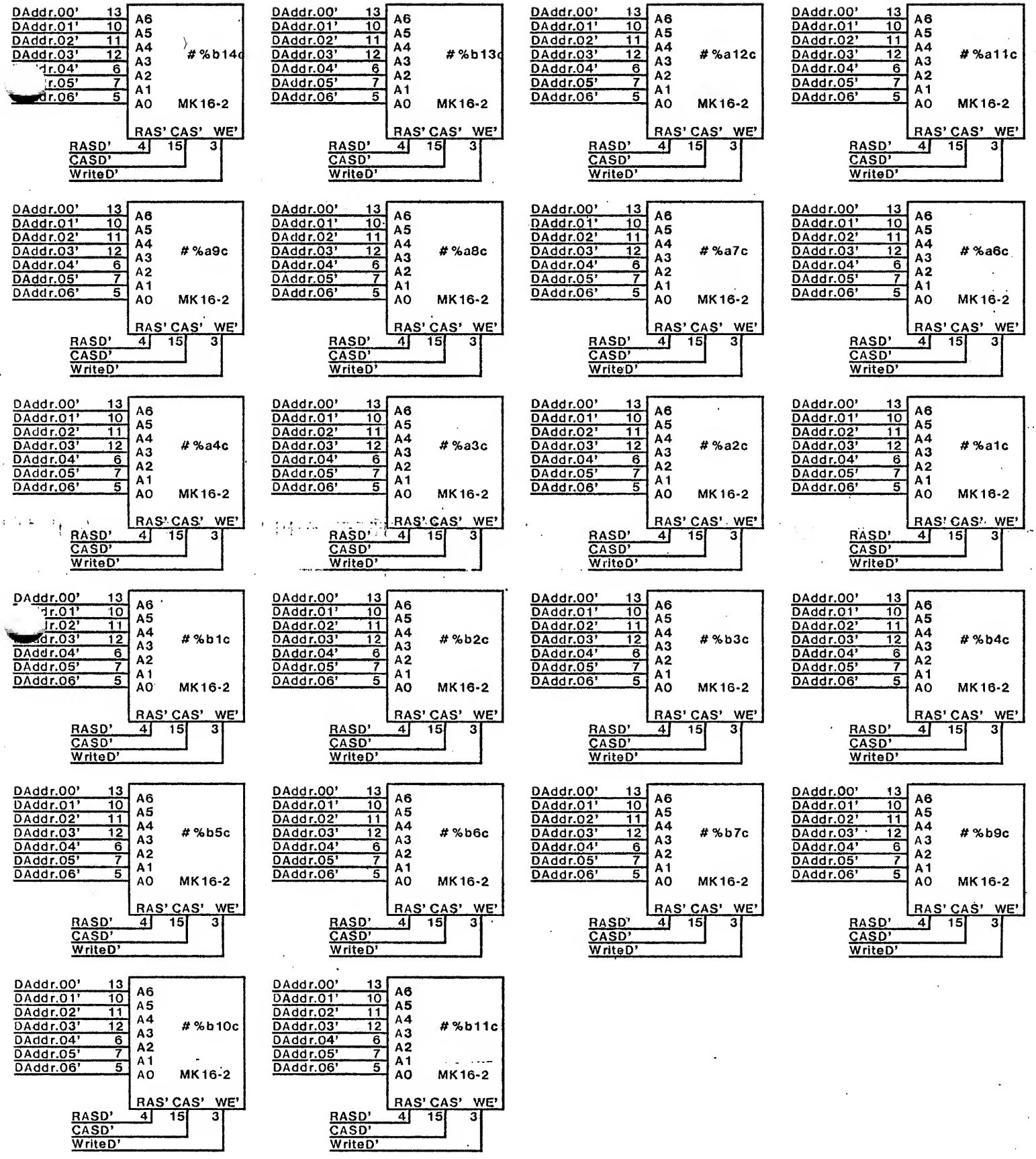
XEROX SDD	Project WS	Mem. Control/ Low Bank A	File EMCTL06.sil	Designer JR Cucinitti	Rev D	Date 2/14/80	Page 6



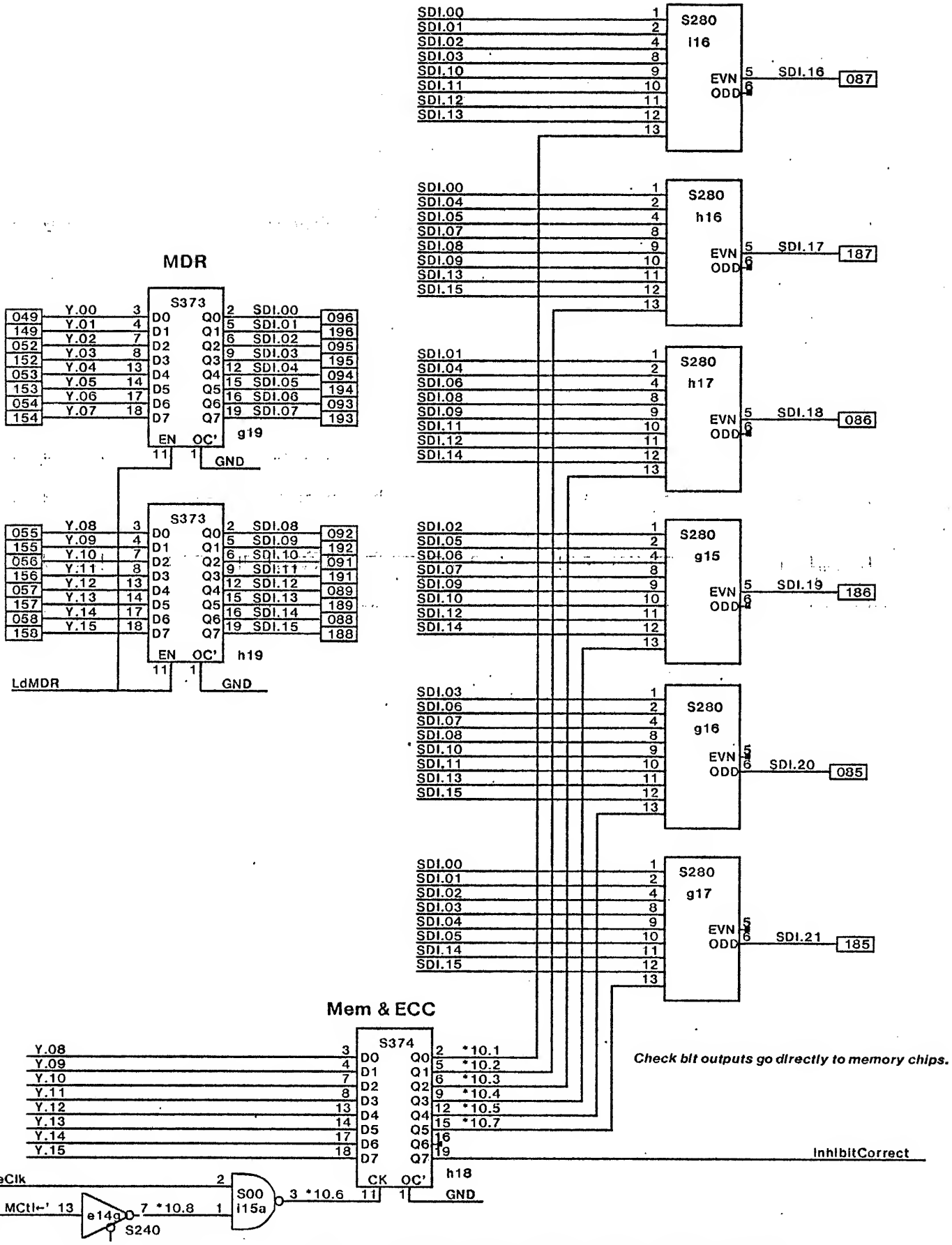
XEROX SDD	Project WS	Mem. Control/ Low Bank B	File EMCTL07.sil	Designer Crane/Cucinitti	Rev D	Date 2/14/80	Page 7



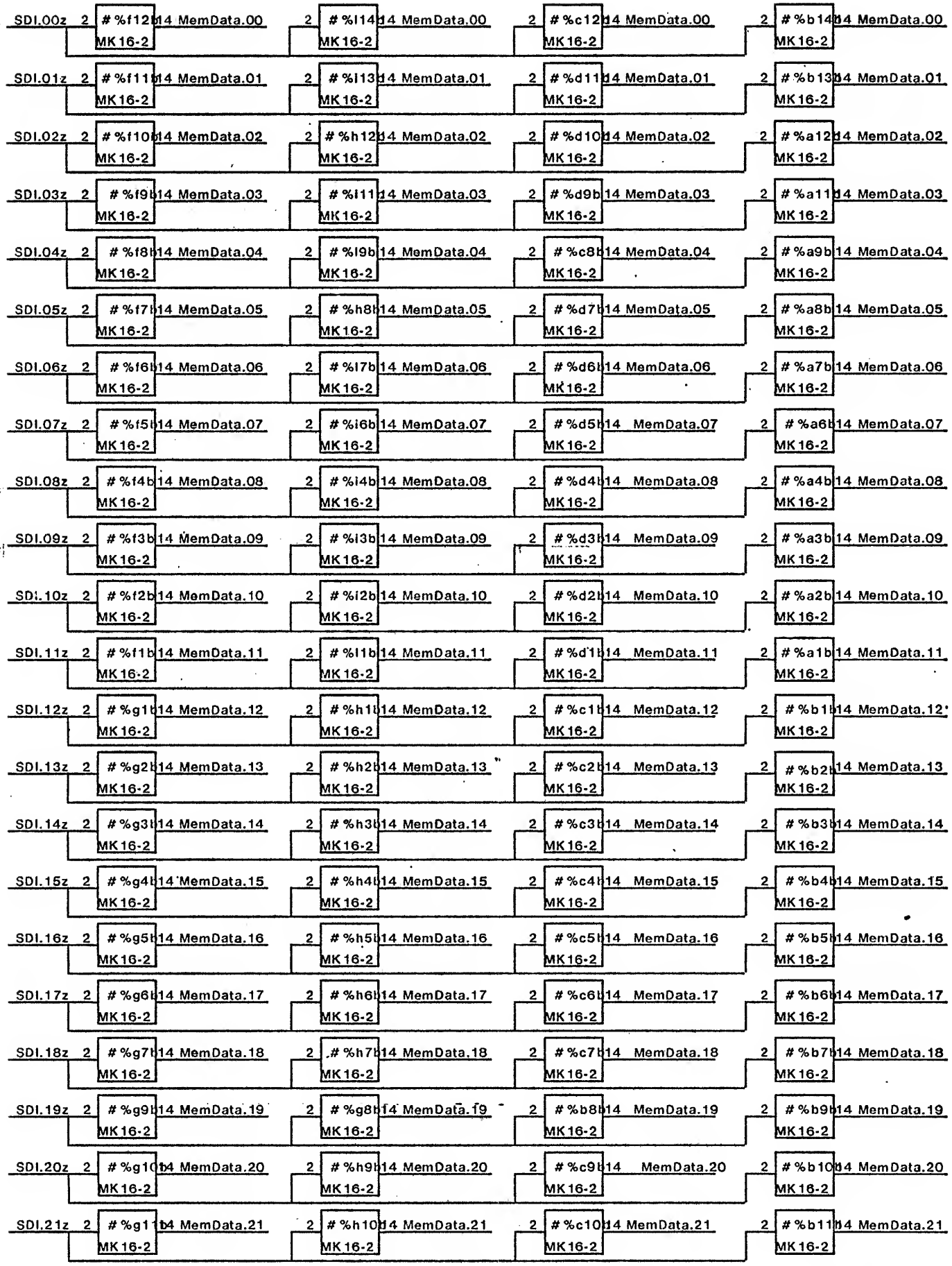
XEROX SDD	Project WS	Mem. Control/ Low Bank C	File EMCTL08.sil	Designer Crane/Cucinitti	Rev D	Date 2/14/80	Page 8



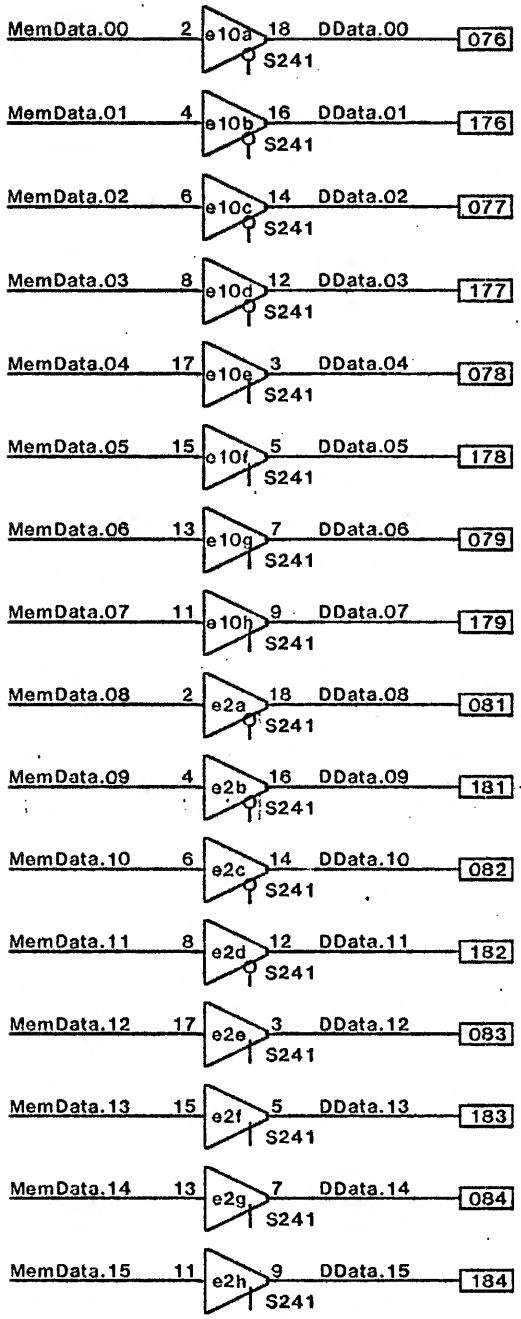
XEROX SDD	Project WS	Mem. Control/ Low Bank D	File EMCTL09.sil	Designer Crane/Cucinitti	Rev D	Date 2/14/80	Page 9



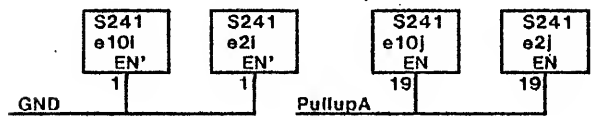
XEROX SDD	Project WS	Mem. Data Reg., Mem. Ctl. Reg. & Check Bit Generator	File EMCTL10.sil	Designer Crane	Rev D	Date 2/14/80	Page 10

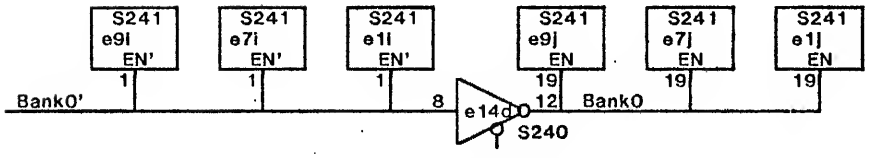


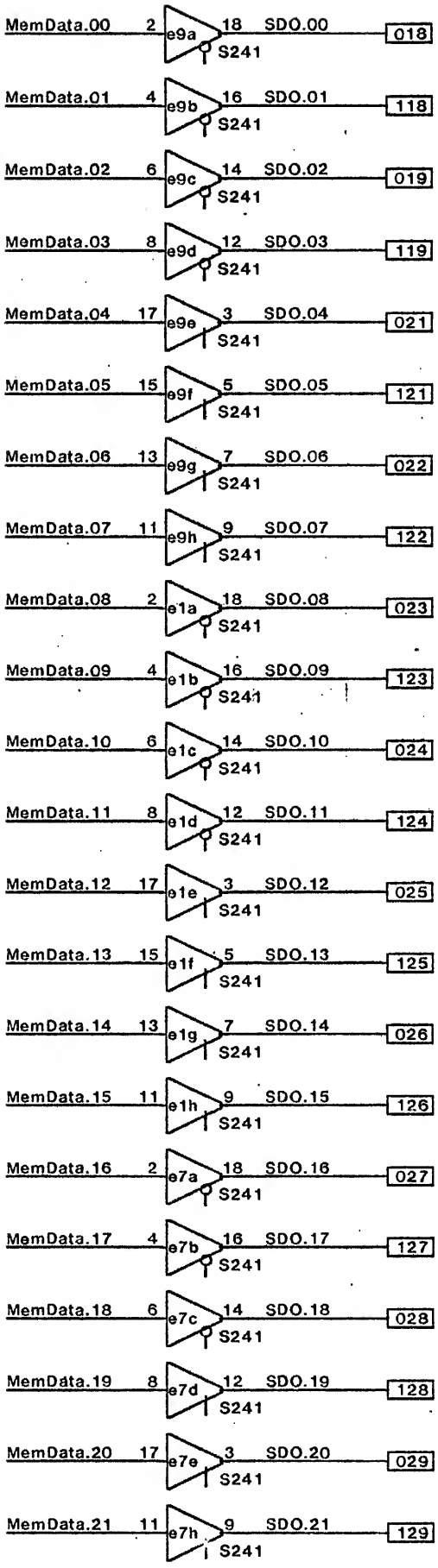
XEROX SDD	Project WS	Work Station Memory Bank0	File EMCTL11.sil	Designer Crane/Cucinitti	Rev D	Date 2/14/80	Page 11



Display Data Buffers

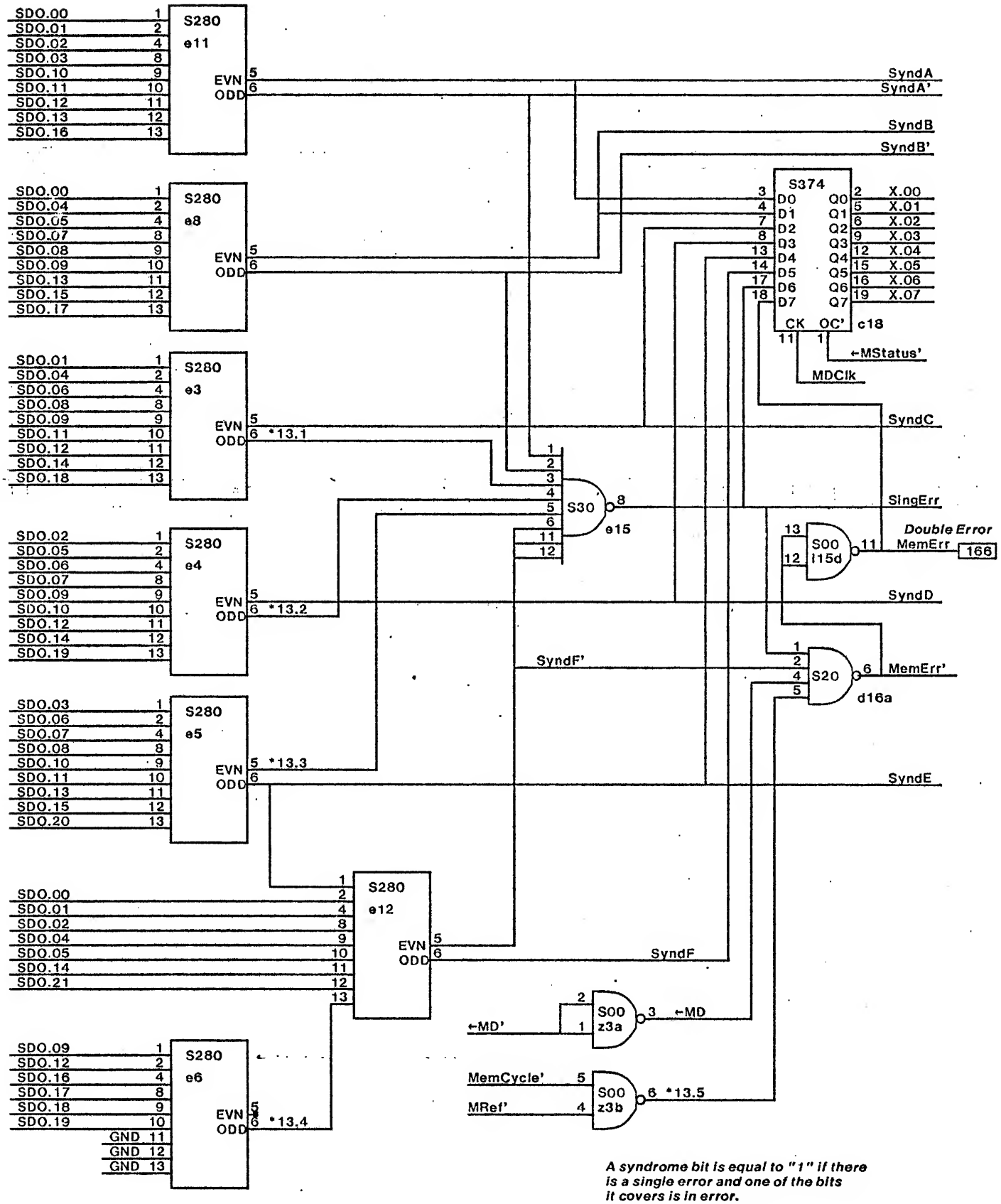






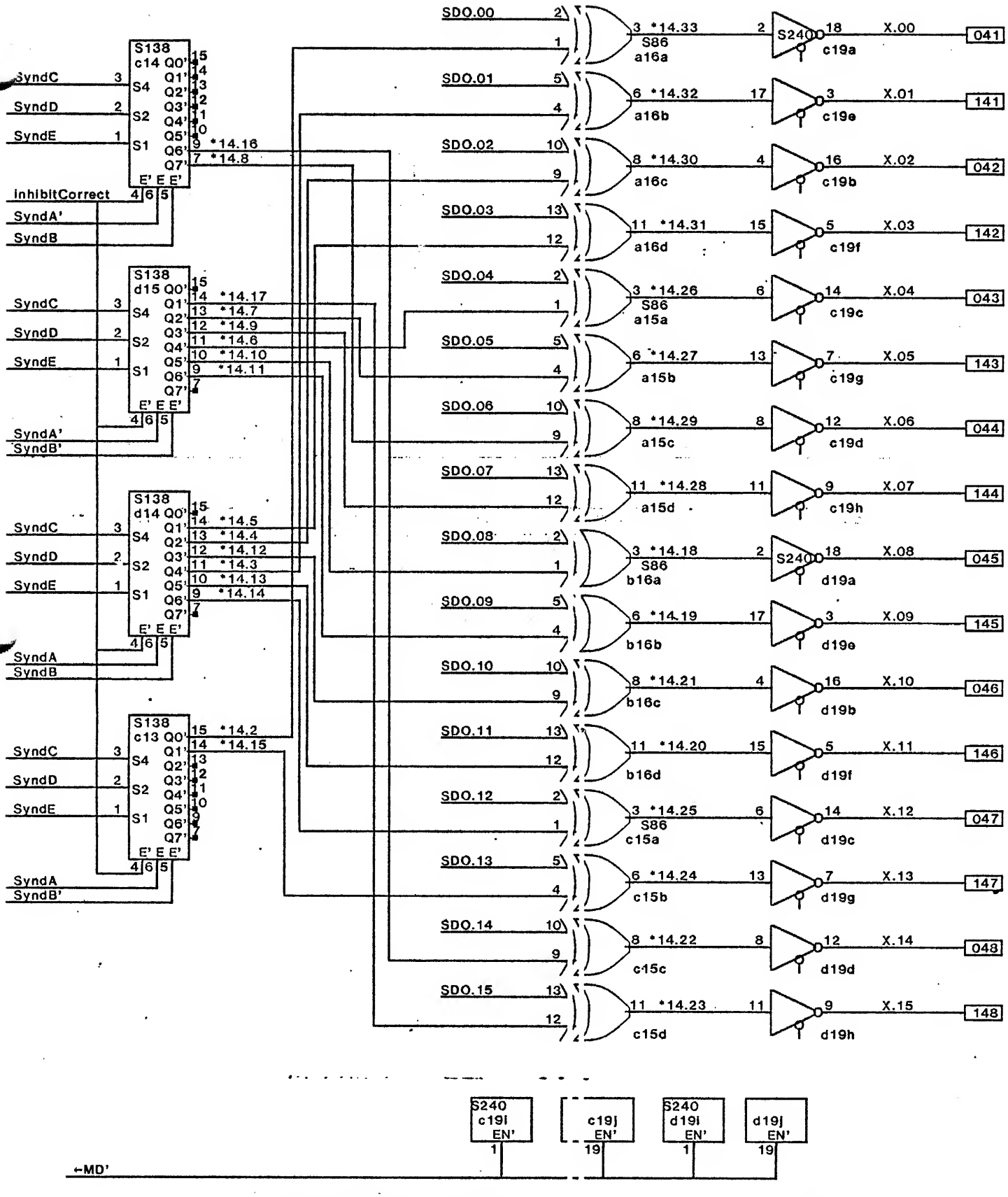
Main Data Buffers

XEROX SDD	Project WS	Data Buffers Low Memory Bank	File EMCTL12.sil	Designer Crane/Cucinitti	Rev D	Date 3/19/80	Page 12



A syndrome bit is equal to "1" if there is a single error and one of the bits it covers is in error.
Syndrome bits A-E point to the bad bit.

XEROX SDD	Project WS	Syndrome Generator	File EMCTL13.sil	Designer Crane	Rev D	Date 2/14/80	Page 13

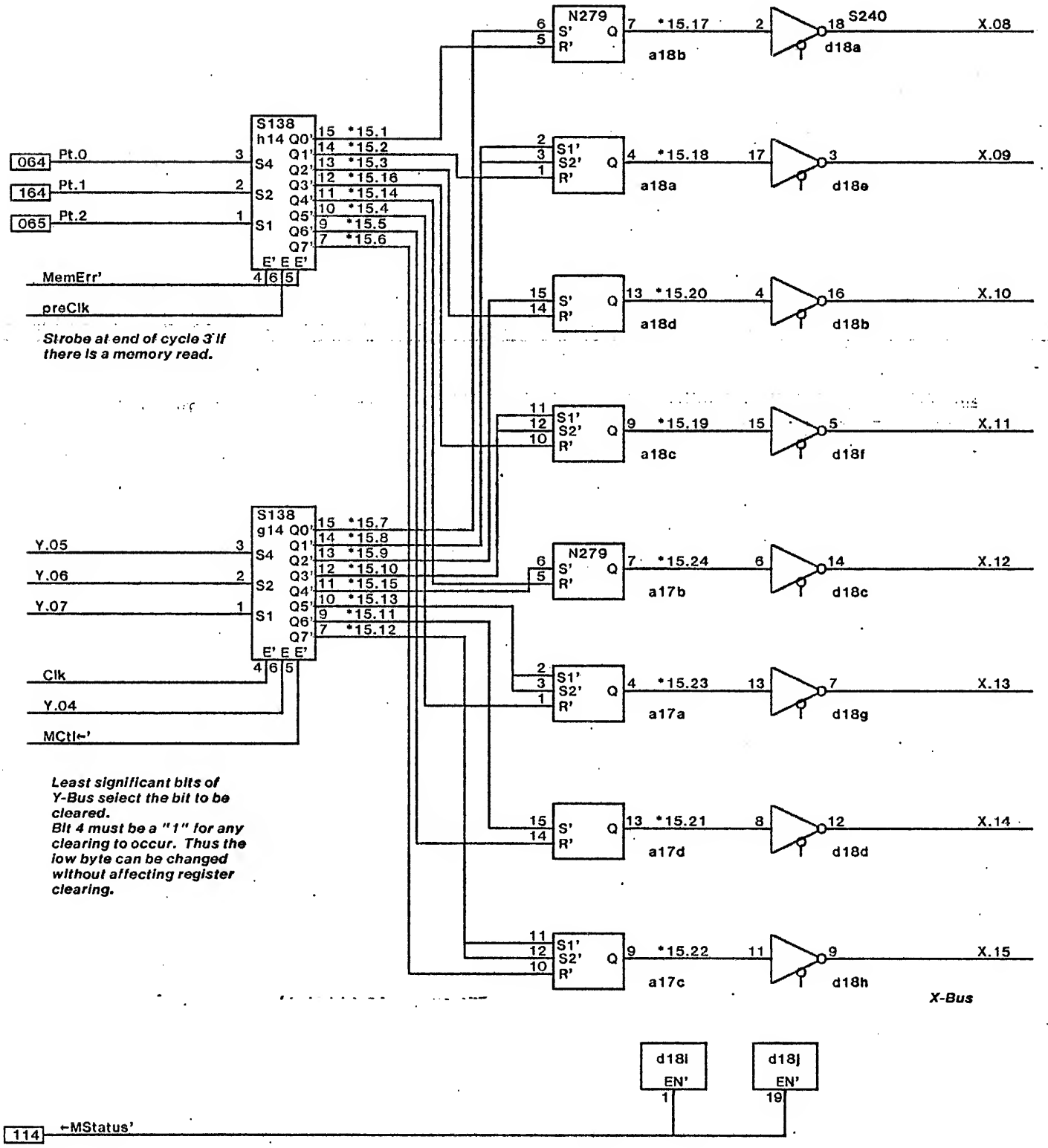


Syndrome Bits point to the bad bit. SyndA is most significant bit & SyndE is LSB.
Syndrome bit is a '1' if one of the bits it covers is in error.

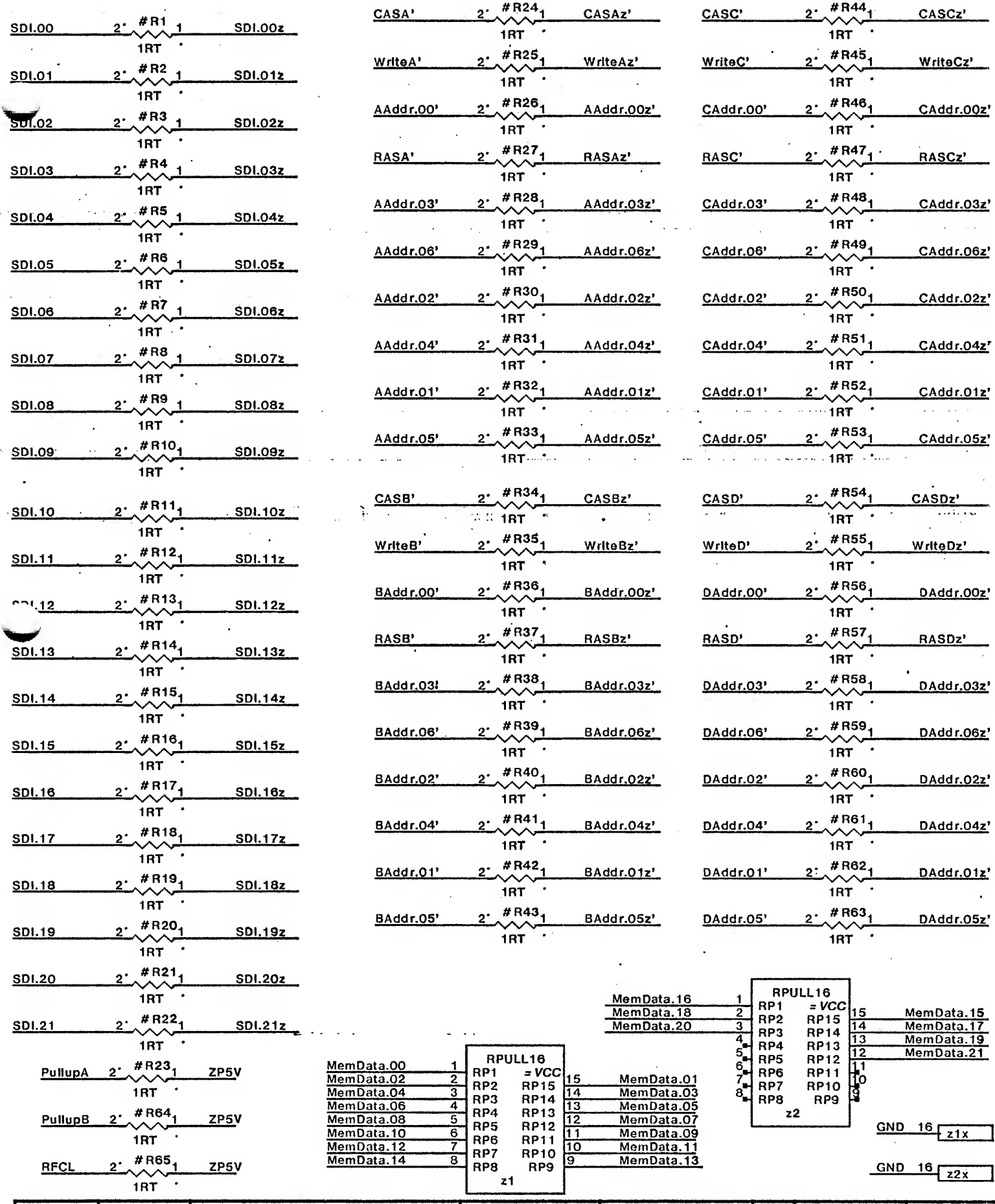
XEROX SDD	Project WS	Error Correction Data Paths	File EMCTL1.41.sil	Designer Crane	Rev D	Date 2/14/80	Page 14

Errors Register

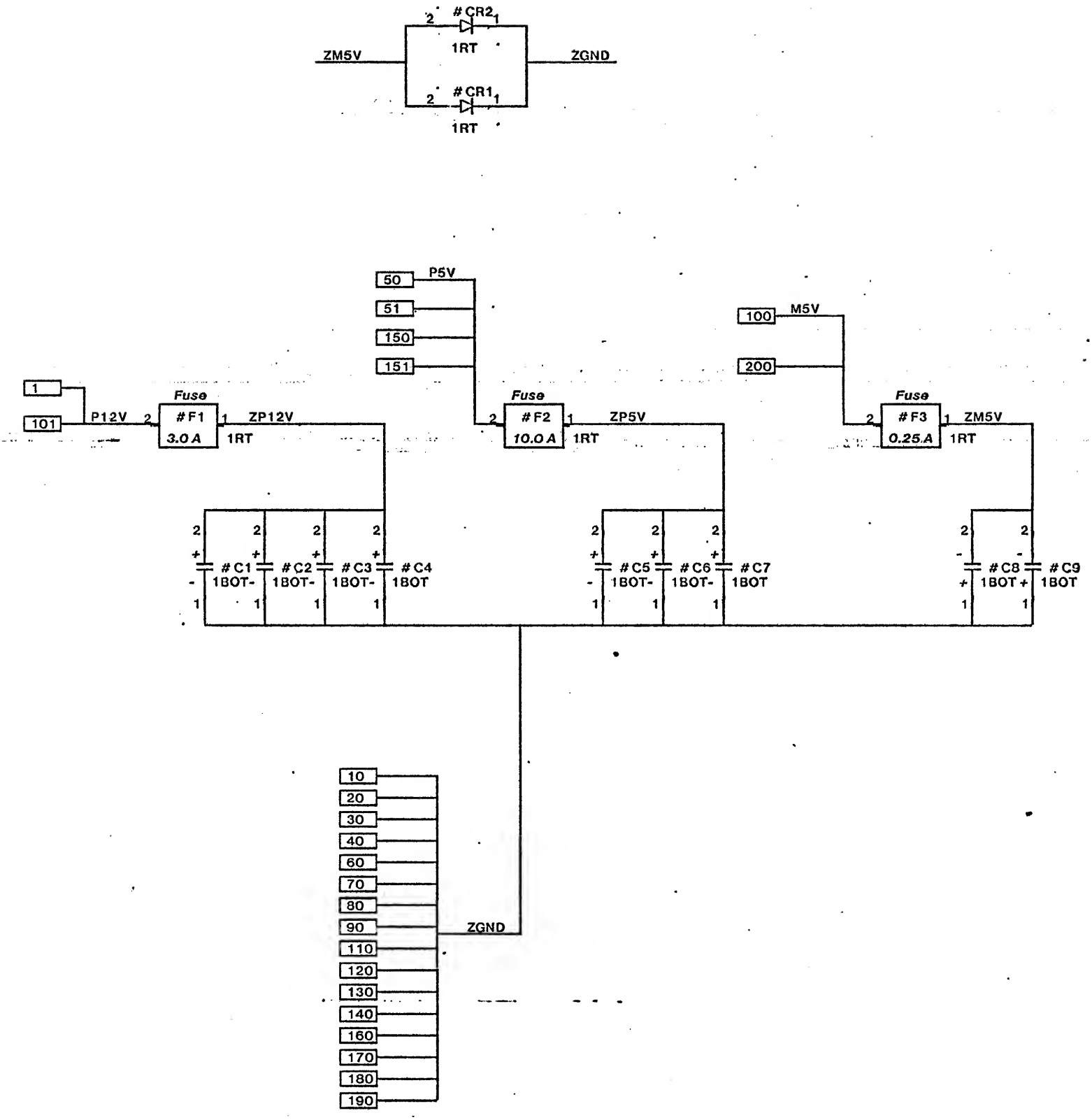
Bit is 1 if there was an error.



XEROX SDD	Project WS	Error Log Register	File EMCTL15.sil	Designer Crane	Rev D	Date 2/14/80	Page 15



XEROX SDD	Project WS	RESISTORS AND R - DIPS	File EMCTL16.sil	Designer Crane/Cucinitti	Rev D	Date 2/14/80	Page 16



XEROX SDD	Project WS	CAPS, DIODES and FUSES	File EMCTL17.sil	Designer Crane/Cucinitti	Rev D	Date 2/14/80	Page 17

CASA' 1 tl #TP001
WriteA' 1 tl #TP002
AAddr.00' 1 tl #TP003
RASA' 1 tl #TP004
AAddr.03' 1 tl #TP005
AAddr.06' 1 tl #TP006
AAddr.02' 1 tl #TP007
AAddr.04' 1 tl #TP008
AAddr.01' 1 tl #TP009
AAddr.05' 1 tl #TP010

CASB' 1 tl #TP011
WriteB' 1 tl #TP012
BAddr.00' 1 tl #TP013
RASB' 1 tl #TP014
BAddr.03' 1 tl #TP015
BAddr.06' 1 tl #TP016
BAddr.02' 1 tl #TP017
BAddr.04' 1 tl #TP018
BAddr.01' 1 tl #TP019
BAddr.05' 1 tl #TP020

CASC' 1 tl #TP021
WriteC' 1 tl #TP022
CAddr.00' 1 tl #TP023
RASC' 1 tl #TP024
CAddr.03' 1 tl #TP025
CAddr.06' 1 tl #TP026
CAddr.02' 1 tl #TP027
CAddr.04' 1 tl #TP028
CAddr.01' 1 tl #TP029
CAddr.05' 1 tl #TP030

CASD' 1 tl #TP031
WriteD' 1 tl #TP032
DAddr.00' 1 tl #TP033
RASD' 1 tl #TP034
DAddr.03' 1 tl #TP035
DAddr.06' 1 tl #TP036
DAddr.02' 1 tl #TP037
DAddr.04' 1 tl #TP038
DAddr.01' 1 tl #TP039
DAddr.05' 1 tl #TP040

SDI.00z 1 tl #TP041
SDI.01z 1 tl #TP042
SDI.02z 1 tl #TP043
SDI.03z 1 tl #TP044
SDI.04z 1 tl #TP045
SDI.05z 1 tl #TP046
SDI.06z 1 tl #TP047
SDI.07z 1 tl #TP048
SDI.08z 1 tl #TP049
SDI.09z 1 tl #TP050
SDI.10z 1 tl #TP051
SDI.11z 1 tl #TP052
SDI.12z 1 tl #TP053
SDI.13z 1 tl #TP054
SDI.14z 1 tl #TP055
SDI.15z 1 tl #TP056
SDI.16z 1 tl #TP057
SDI.17z 1 tl #TP058
SDI.18z 1 tl #TP059
SDI.19z 1 tl #TP060
SDI.20z 1 tl #TP061
SDI.21z 1 tl #TP062

MCycle 1 tl #TP085

LatchY.02 1 tl #TP086
LatchY.03 1 tl #TP087
LatchY.05 1 tl #TP088
LatchY.06 1 tl #TP089
LatchY.07 1 tl #TP090
LatchY.08 1 tl #TP091
LatchY.09 1 tl #TP092
LatchY.10 1 tl #TP093
LatchY.11 1 tl #TP094
LatchY.13 1 tl #TP095
LatchY.14 1 tl #TP096
LatchY.15 1 tl #TP097

MemData.00 1 tl #TP063
MemData.01 1 tl #TP064
MemData.02 1 tl #TP065
MemData.03 1 tl #TP066
MemData.04 1 tl #TP067
MemData.05 1 tl #TP068
MemData.06 1 tl #TP069
MemData.07 1 tl #TP070
MemData.08 1 tl #TP071
MemData.09 1 tl #TP072
MemData.10 1 tl #TP073
MemData.11 1 tl #TP074
MemData.12 1 tl #TP075
MemData.13 1 tl #TP076
MemData.14 1 tl #TP077
MemData.15 1 tl #TP078
MemData.16 1 tl #TP079
MemData.17 1 tl #TP080
MemData.18 1 tl #TP081
MemData.19 1 tl #TP082
MemData.20 1 tl #TP083
MemData.21 1 tl #TP084

RFCL 1 tl #TP098

PullupB 1 tl #TP099

XEROX SDD	Project WS	TEST POINTS	File EMCTL18.sil	Designer Crane/Cucinitti	Rev D	Date 3/19/80	Page 18

ITEM	DESCRIPTION			DWG #	QTY	REMARKS
1	INTEGRATED CIRCUIT	SN74S00		733w00318	3	
2	INTEGRATED CIRCUIT	SN74S02		733w01643	3	
3	INTEGRATED CIRCUIT	SN74S04		733w00319	1	
4	INTEGRATED CIRCUIT	SN74S10		733w01606	3	
5	INTEGRATED CIRCUIT	SN74S20		733w01619	1	
6	INTEGRATED CIRCUIT	SN74S30		733w01645	1	
7	INTEGRATED CIRCUIT	SN74S37		733w02136	1	
8	INTEGRATED CIRCUIT	SN74S74		733w01771	2	
9	INTEGRATED CIRCUIT	SN74S86		733w01648	4	
10	INTEGRATED CIRCUIT	SN74S138		733w01616	6	
11	INTEGRATED CIRCUIT	SN74S139		733w01669	1	
12	INTEGRATED CIRCUIT	SN74S240		733w01633	9	
13	INTEGRATED CIRCUIT	SN74S241		733w01634	5	
14	INTEGRATED CIRCUIT	SN74S253		733w01636	8	
15	INTEGRATED CIRCUIT	SN74279		733w00341	2	
16	INTEGRATED CIRCUIT	SN74S280		733w01638	13	
17	INTEGRATED CIRCUIT	SN74S373		733w01699	4	
18	INTEGRATED CIRCUIT	SN74S374		733w01640	2	
19	INTEGRATED CIRCUIT	SN74LS393		733w01663	1	
20	MEMORY CHIP 16K	MK4116-2		733w01512	88	
21	CAPACITOR	0.1uf 50v		102P20600	115	
22	CAPACITOR	20uf 15v		702W07301	5	C5 --> C9 (alt. 25uf 12v 702W05601)
23	CAPACITOR	10uf 25v		702W08901	4	C1 --> C4
24	DELAY LINE	25 ns	Eng Components Co.	744W00001	2	X1 + X2 TTLDM025
25	DIODE	1N5820		107P10105	2	CR1 + CR2
26	FUSE	0.25 A		708W10302	1	F3
27	FUSE	3.0 A		708W11002	1	F1
28	FUSE	10.0 A		708W11402	1	F2
29	R-DIP	1.0 k ohm		703W13291	2	Z1 + Z2
30	RESISTOR	18 ohm	1/4 watt 5 %	703W28088	12	R24,R25,R27,R34,R35,R37,R44,R45, R47,R54,R55 + R57
31	RESISTOR	20 ohm	1/4 watt 5 %	703W28188	28	R26,R28 --> R33,R36,R38 --> R43, R46,R48 --> R53,R56,R58 --> R63
32	RESISTOR	27 ohm	1/4 watt 5 %	703W28488	22	R1 --> R22
33	RESISTOR	1.0 k ohm	1/4 watt 5 %	703W32288	3	R23,R64 + R65
34	PWB			140P11229	1	
35	BOARD EXTRACTOR			003P80513	2	
36	STIFFENER	(front)		596P54167	1	
37	STIFFENER	(back)		030P83244	1	
38	RIVETS			320W13201	7	

Error Correction Logic

Code Table

The codes have been optimized for use with 9 input parity chips (S280). Each row represents the inputs to a single chip. 8 inputs are used when writing and 9 are used when reading.

(Check bit F is parity over entire word. X's are omitted from the group of bits whose overall parity remains fixed.)

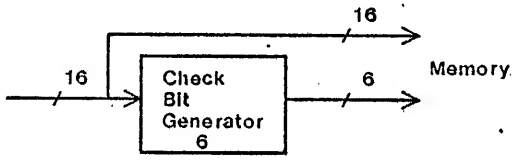
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	a	b	c	d	e	f
a	x	x	x	x							x	x	x	x			x					
b	x				x	x		x	x	x				x		x		x				
c		x			x		x		x	x		x	x		x				x			
d			x			x	x	x		x	x		x		x					x		
e				x			x	x	x		x	x		x		x					x	
Parity over all 22 bits f	x	x	x	x	x	x									x	x						x

Data Bits | Check Bits

Writing

Check bits written into memory are parity calculated over the data bits in the corresponding row.

Check bits a-d are odd parity and bits e-f are even parity. Bit f is really parity over the whole word, but the number of bits directly used to generate bit F is only 8 since the other data bits are cancelled out by other check bits.

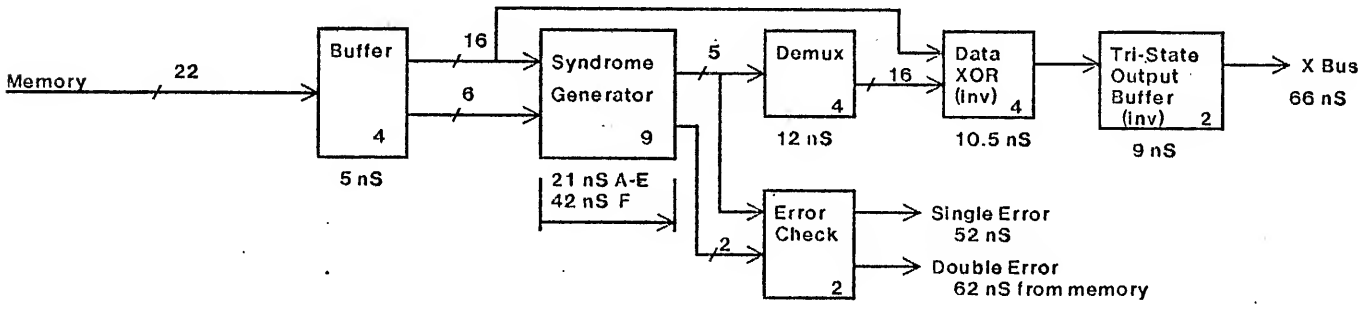


Parity checker chips
Delay = 1.15 (21) = 24 nS

Reading

All bits from rows A-E are used for the corresponding syndrome bit. (Stored parity: A-D = odd, E,F = even)

All 22 bits of the stored memory word are included in generation of syndrome bit F.



Numbers inside boxes are the number of chips used for the function.

Numbers below boxes are maximum delays from TI TTL Data book. 15% is added below to allow for board propagation time

Total Delay for Data = 1.15 (57.5) = 66 nS or 61 nS without buffer

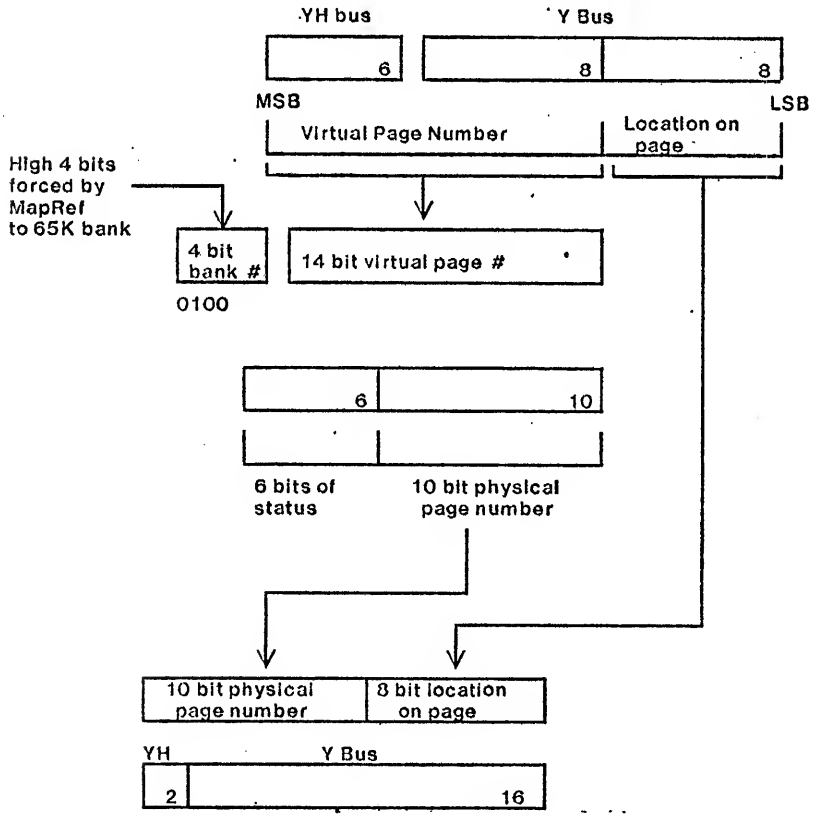
Error Check Possibilities

Syndrome		Meaning
OR A-F	Synd F	
0	0	No error or >2 errors
0	1	Not Possible
1	0	Dbl error detected
1	1	Single error corrected

Map References

The memory system supports a 22 bit virtual address space divided into pages of 256 words each. Thus, 14 bits specify the page number and 8 bits specify the location within the page.
The physical memory system will support up to 256K of real memory, i.e. an 18 bit address space. Thus there is a 10 bit physical page number and 8 bits as above for specifying the location within the page.
Since the virtual space is larger than the physical space, a mapping is performed between the 14 bit virtual page number and the 10 bit physical page number. The 14 bit virtual page number is used to access one of 16K locations which comprise the map in main memory. The accessed memory location (map entry) contains the 10 bit physical page number and status bits for the page (write protect, referenced, dirty).

Map References to the memory system are done by specifying MapRef in the microcode and sending the 22 bit virtual memory address to the memory via the Y (16 bits) and YH (6 bits) busses.
This causes an access into the map, a 16K word segment of main memory located between 65K and 80K. Specifying MapRef forces access to the 65K-80K bank while the high 14 bits of the 22 bit virtual address are used to access a word within that 16K bank.



22 bit virtual address delivered to memory

18 bit physical address accessed in memory

Contents of Map Entry

Status Bits
- Dirty
- Referenced
- Write Protect
  - Not Present = (dirty & writeprotect)
- 3 extra bits

Microcode concatenates 10 bit physical page number to 8 bit locaton on page to produce 18 bit physical address.

The 18 bit physical address is delivered to the memory on the Y and YH busses.